Claims

[c1] 1.A method of fabricating a trench flash memory device, comprising:
providing a substrate which has a upper surface;
forming a patterned mask layer on the substrate;
forming a trench in the substrate by using the patterned mask layer as a mask;
forming a source region in the substrate around the bottom of the trench;
forming a tunnel oxide layer in the trench;
forming a first conductive layer in the trench wherein the first conductive layer has a top surface below the upper surface of the substrate.
forming a gate dielectric layer over the first conductive layer;
forming a second conductive layer, where the second conductive layer completely fills the trench;
removing the second conductive layer and the gate dielectric layer outside the trench to expose the patterned mask layer;
removing the exposed patterned mask layer to expose the substrate; and
forming a drain region in the substrate, wherein the drain region is adjacent to a top portion of the trench.

[c2] 2.The method of claim 1, wherein forming the source region in the substrate further comprises:
forming a conformal doped insulating layer in the trench;
forming a first photo-resist layer around the bottom of the trench, which the first photo-resist layer does not fully fill the trench and leaves part of the doped insulating layer exposed;
removing the doped insulating layer which is not covered by photo-resist, leaving the doped insulating layer around the bottom of the trench untouched;
removing the first photo-resist layer;
forming a cap layer on the side wall of the trench;
performing a thermal process to drive the dopant in the doped insulating layer into the surrounding area and form the source region; and
removing the doped insulating layer near the bottom of the trench and the cap layer on the sidewall of the trench.

[c3] 3.The method of claim 2, wherein the material of the doped insulating layer is

Arsenic ion doped silicon oxide.

[c4] 4.The method of claim 1, wherein the step of forming the first conductive layer comprises the steps of:
depositing a conductive layer on the surface of the trench and the substrate;
forming a second photo-resist layer, which does not fully fill the trench and expose a part of the conductive layer;
removing part of the conductive layer which is not covered by the second photo-resist layer; and
removing the second photo-resist layer to form the first conductive layer.

[c5] 5.The method of claim 1, wherein the method further comprises a repairing process after the formation of the source region in the substrate around the bottom of the trench and before the formation of the tunnel oxide layer.

[c6] 6.The method of claim 5, wherein the repairing process comprises the steps of:
performing a thermal process to form a liner oxide layer on the side wall of the trench and the substrate surface; and
Removing the liner oxide layer.

[c7] 7.The method of claim 1, wherein the method further comprises the steps of:
forming a first well region having a first conduction type in the substrate, wherein the first well region connects with the source region;
forming a second well region having a second conduction type above the first well region with the first conduction type; and
forming a third well region having the first conduction type in the substrate, which connects the second well region with the second conduction type with the first well region having the first conduction type.

[c8] 8. The method of claim 7, wherein the first well region includes a deep n-type well region.

[c9] 9. The method of claim 7, wherein the second well region includes a p-type well region.

[c10] 10. The method of claim 7, wherein the third well region includes an n-type well

region.

[c11] 11.The method of claim 1, wherein there is a pad oxide layer between the patterned mask layer and the substrate.

[c12] 12.The method of claim 1, wherein is the method further comprises a step of forming an isolation structure in the substrate to define the active area after the step of removing the mask layer to expose the substrate and before the formation of the drain region in the substrate around the top of the trench.

[c13] 13. A trench flash memory device, comprising:
a substrate having a trench;
a gate structure, which is located in the trench and has the following components from outside to inside of the trench: a tunnel oxide layer, a floating gate, a gate dielectric layer and a control gate, wherein the tunnel oxide layer, the floating gate and the gate dielectric layer wrap around the control gate;
a source region, which is located in the substrate around the bottom of the trench; and
a drain region, which is located in the substrate adjacent to the top of the trench.

[c14] 14.The device of claim 13, further comprising:
a first well region having a first conduction type, formed in the substrate and connected with the source region;
a second well region having a second conduction type, formed above the first well region; and
a third well region having the first conduction type formed in the substrate, which connects the second well region with the first well region.

[c15] 15.The device of claim 14, wherein the first well region having the first conduction type includes a deep n-type well region.

[c16] 16.The device of claim 14, wherein the second well region having the second conduction type includes a p-type well region.

[c17] 17.The device of claim 14, wherein the third well region having the first

conduction type includes an n-type well region.

[c18] 18.The device of claim 13, wherein the gate dielectriclayer includes silicon oxide/silicon nitride/silicon oxide layer.

[c19] 19.The device of claim 13, wherein the floating gate has a top surface lower than the upper surface of the substrate.

[c20] 20.The device of claim 13, wherein the control gate has a top surface higher than the upper surface of the substrate.